Serial Number: 09/459703

Filing Date: December 13, 1999

Title: SYSTEM AND METHOD FOR REPRODUCING SYSTEM EXECUTIONS USING A REPLAY

Page 6

Dkt: 884.027ŪS1

HANDLER (AS PREVIOUSLY AMENDED)

Assignee: Intel Corporation

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REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on January 12, 2004, and the references cited therewith.

Claim 10 has been amended, no claims have been added and no claims have been canceled. Thus, claims 1-23 are now pending in this application.

About the Claim Amendments

Applicant has made a claim amendment to correct a grammatical mistake and to more clearly point-out the invention. This amendment was not for reasons of patentability. In particular, a comma was added to separate elements recited in the claim.

\$102 Rejection of the Claims

Claims 1-8, 10, 11, 14-20, 22, and 23 were rejected under 35 USC § 102(e) as being anticipated by Deao et al. (U.S. 5,065,106, hereinafter referred to as Deao). Applicant respectfully traverses this rejection because Deao does not anticipate the claimed invention, as set forth in claims 1-8, 10, 11, 14-20, 22, and 23.

Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *In re Dillon* 919 F.2d 688, 16 USPQ 2d 1897, 1908 (Fed. Cir. 1990) (en banc), cert. denied, 500 U.S. 904 (1991). It is not enough, however, that the prior art reference discloses all the claimed elements in isolation. Rather, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim*." *Lindemann Maschinenfabrik GmbH v. American Hoist &*

Serial Number: 09/459703

Filing Date: December 13, 1999

e: SYSTEM AND METHOD FOR REPRODUCING SYSTEM EXECUTIONS USING A REPLAY

Page 7

Dkt: 884.027US1

HANDLER (AS PREVIOUSLY AMENDED)

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Derrick Co., 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing Connell v. Sears, Roebuck & Co., 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added).

Applicant respectfully submits that the Office Action did not make out a *prima facie* case of anticipation because the reference does not teach each and every element of the rejected claims.

Deao describes a system for debugging and emulating an integrated circuit with an external test system. See Abstract. As shown in Figure 1, the integrated circuit 42 is connected to a test system 51, which is external to the integrated circuit 42. When the system is performing emulation operations, "a sequence of debug instructions is scanned into the multi-word instruction register from external test system 51." Deao Col. 51, lines 62-64. According to Deao, in response to an emulation event, the processor executes the sequence of debug instructions. See Deao Col. 51, lines 57-64. Once "the debug operations are done, test system 51 restores the saved state of the instruction execution pipeline." Deao Col. 52, lines 7-9. In other words, Deao's sequence of debug instructions executes just once in response to a single emulation event. Deao's sequence of debug instructions can be triggered again, but this requires another emulation event. See Deao Col 52, lines 4-6.

Independent claim 1 teaches a processor "configured to test itself by *repeatedly* executing a plurality of instructions using a replay handler" (emphasis added). The remaining claims rejected under §102 recite a similar replay handler that repeatedly replays system executions. See claims for the exact language. The Office Action asserts that Deao's "sequence of debug instructions is the replay/restart handler". However, the claimed replay handler is altogether different from Deao's sequence of emulation-event-triggered debug instructions. Although the

Serial Number: 09/459703

Filing Date: December 13, 1999

SYSTEM AND METHOD FOR REPRODUCING SYSTEM EXECUTIONS USING A REPLAY

HANDLER (AS PREVIOUSLY AMENDED)

Assignee: Intel Corporation

replay handler requires an initial replay break to begin execution, the replay handler does not require another replay break or emulation event to execute the replay handler again. "The replay handler may have a predetermined number of replays for each execution." Specification at page 7, lines 21-23. That is, the claimed replay handler will repeatedly execute as many times as were predetermined before the replay break. Because the claimed replay handler will repeatedly execute without another emulation event, Deao does not teach a replay handler, as recited in the rejected claims.

In addition to the assertions noted above, Applicant submits that the rejected claims are patentable for the reasons set forth in the previous response. See Response mailed January 12, 2004. The Office Action rejects Applicant's previous assertions on the basis that Deao's "multiword register is part of the memory hierarchy." Applicant respectfully disagrees and submits that the Office Action has mischaracterized a multi-word register as being part of the memory hierarchy. "The memory hierarchy 102 can be an amount of dynamic ram, cache memory, a linear array, or virtual memory." Specification at page 4, lines 12-13. However, registers (which are not DRAM, cache memory, linear array or virtual memory) are not part of the memory hierarchy.

Applicant respectfully submits that rejected claims 1-8, 10, 11, 14-20, 22, and 23 are patentable for at least the reasons discussed above and the elements of the claims. As such, Applicant respectfully requests that the rejections under 35 USC § 102(e) be withdrawn.

Page 8 Dkt: 884.027US1

Serial Number: 09/459703

Filing Date: December 13, 1999

le: SYSTEM AND METHOD FOR REPRODUCING SYSTEM EXECUTIONS USING A REPLAY

Page 9 Dkt: 884.027US1

HANDLER (AS PREVIOUSLY AMENDED)

Assignee: Intel Corporation

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§103 Rejection of the Claims

Claims 9, 12, 13, and 21 were rejected under 35 USC § 103(a) as being unpatentable over US Patent No. 6,065,106 (referred to herein as Deao). Applicant respectfully traverses this rejection because the Office Action has not established a *prima facie* case of obviousness regarding the claims noted above.

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). To do that the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would lead an individual to combine the relevant teaching of the references. *Id*.

The *Fine* court stated that:

Obviousness is tested by "what the combined teaching of the references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 878 (CCPA 1981)). But it "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." *ACS Hosp. Sys.*, 732 F.2d at 1577, 221 USPQ at 933. And "teachings of references can be combined *only* if there is some suggestion or incentive to do so." *Id.* (emphasis in original).

The M.P.E.P. adopts this line of reasoning, stating that

In order for the Examiner to establish a prima facie case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. M.P.E.P. § 2142 (citing In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir. 1991)).

Serial Number: 09/459703

Filing Date: December 13, 1999

Fitle: SYSTEM AND METHOD FOR REPRODUCING SYSTEM EXECUTIONS USING A REPLAY

Page 10

Dkt: 884.027US1

HANDLER (AS PREVIOUSLY AMENDED)

Assignee: Intel Corporation

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Dependent claims 9, 12, 13, and 21 depend directly or indirectly from independent claims 6, 10, and 20. Because the rejection under 35 USC §103 does not provide any teaching or suggestion about how one of ordinary skill in the art would modify Deao to make the claimed invention, Applicant respectfully submits that dependent claims 9, 12, 13, and 21 are patentable over Deao for at least the reasons given above, with reference to claims 6, 10, and 20.

Reservation of Rights

Applicant does not admit that references cited under 35 U.S.C. §§ 102(a), 102(e), 103/102(a), or 103/102(e) are prior art, and reserves the right to swear behind them at a later date. Arguments presented to distinguish such references should not be construed as admissions that the references are prior art.

NDMENT AND RESPONSE UNDER 37 CFR § 1.111 ial Number: 09/459703

Page 11 Dkt: 884.027US1

Filing Date: December 13, 1999

SYSTEM AND METHOD FOR REPRODUCING SYSTEM EXECUTIONS USING A REPLAY

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Intel Corporation Assignee:

Conclusion

Based on the foregoing, Applicant respectfully requests that the rejections be withdrawn. Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 371-2169 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

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By his Representatives,

Respectfully submitted,

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Date _	9-12-04	By	
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Non-Fee Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 12th day of April 2004

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Name

Signature